REMARKS/ARGUMENTS

STATUS OF CLAIMS

In response to the Office Action dated September 21, 2007, claims 2 and 3 have been amended. Claims 2-5, 7, 8, 10 and 11 are now pending in this application. No new matter has been added.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 103

I. Claims 1-3 and 6-11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Azuma et al. (Embedded Anti-Aliasing in Switched-Capacitor Ladder Filters With Variable Gain and Offset Compensation, IEEE Journal of Solid-State Circuits, Vol. 37, No. 3, March 2002, Pages 349-356) in view of Bonaccio et al. (U.S. Patent No. 6,034,568). However, it is believed that the Examiner intended claims 2, 3, 7, 8, 10 and 11 since claims 1, 6 and 9 are not pending in this application.

The Examiner contends that Azuma et al. discloses the inventions of claims 2 and 3 except that at least one of the integration circuits includes a bipolar transistor. However, the Examiner maintains that "it is notoriously known in the art that the operational amplifiers of Azuma et al. may be constructed of bipolar or FET".

In the Response to Amendment/Argument at page 2 of the Office Action, the Examiner asserts:

> The Applicant argues that, supposedly in contrast to the prior art combination, "the switched capacitor filter of the subject application is, as shown in Figs. 1 and 2, arranged such that the transistor on the input (first) stage of the amplifier is a bipolar transistor, whereas the other transistors are FET transistors."

(pg. 8.) However, the prior art combination does not necessarilty suggest replacing all operation amplifiers of Azuma with bipolar amplifiers. Furthermore, although Applicant notes that figure 1 illustrates a first stage bipolar amplifier (fig. 1, ref. 104) and remaining stages of FET amplifiers (fig 1, refs,. 102 and 103) to distinguish from the prior art of record, none of the claims contain such express limitations.

To expedite prosecution, independent claim 2 has been amended to recite:

A switched capacitor filter having an anti-aliasing function, comprising:
integration circuits of multiple stages, each having an amplifier and a switched capacitor, wherein
the integration circuit of at least a first stage of the integration circuits of multiple stages has a resistor,
a bipolar transistor is provided in an input stage of the amplifier in at least ***the first stage*** of the integration circuits ***of multiple stages,***
no bipolar transistor is provided in the input stage of the amplifier of any integration circuit, of the integration circuits of multiple stages, that does not have a resistor, and
any amplifier that does not have the bipolar transistor provided in the input stage is provided with a metal-oxide-semiconductor field-effect-transistor (MOSFET) instead.

In addition, independent claim 3 has been amended to recite:

A switched capacitor filter having an anti-aliasing function, comprising:
integration circuits of multiple-stages, each having an amplifier and a switched capacitor, wherein
an integration circuit of at least a first stage of the integration circuits of multiple stages has a resistor,
the integration circuits each has a distributed gain so as to maintain a filtering function in each of the multiple-stages of integration circuits,
a bipolar transistor is provided in an input stage of ***the*** amplifier ***in the first stage of the integration circuits of multiple stages, as well as in the input stage of the amplifier in other stages*** which ***show*** a strong 1/f noise reduction effect ***by using the bipolar transistor, and***
any amplifier that does not have the bipolar transistor provided in the input stage is provided with a metal-oxide-semiconductor field-effect-transistor (MOSFET) instead.

Thus, the invention recited in independent claim 2 is different from Bonaccio et al. because there is no disclosure or suggestion that no bipolar transistor is provided in the input stage of the amplifier of any integration circuit, of the integration circuits of multiple stages, that does NOT have a resistor, and any amplifier that does not have the bipolar transistor provided in the input stage is provided with a metal-oxide-semiconductor field-effect-transistor (MOSFET) instead (claim 2). The Examiner maintains that Bonaccio et al. teaches "FET-input operational amplifiers suffer from larger initial offsets and much larger drifts of offset voltage with temperature deviations than do bipolar transistor operational amplifiers". If this teaching were applied, as suggested by the Examiner, i.e., "one skilled in the art, in accordance with Bonaccio's teaching, would choose operational amplifiers comprised completely of bipolar transistors as they are well known in the art", all the integration circuits of multiple stages of Azuma et al. would have bipolar transistors, including integration circuits that do NOT have a resistor (see elements 2 and 3 of Fig. 1of Azuma et al.

Furthermore, the invention recited in independent claim 3 is different from Bonaccio et al. because a bipolar transistor is provided in an input stage of the amplifier in the first stage of the integration circuits of multiple stages, as well as in the input stage of the amplifier in other stages which show a strong 1/f noise reduction effect by using the bipolar transistor, and any amplifier that does not have the bipolar transistor provided in the input stage is provided with a metal-oxide-semiconductor field-effect-transistor (MOSFET) instead (claim 3).

Thus, amended independent claims 2 and 3 are patentable over Azuma et al. and Bonaccio et al., as are claims 7, 8, 10 and 11. Therefore, the allowance of claims 2, 3, 7, 8, 10 and 11, as amended, is respectfully solicited.

II. Claims 4 and 5 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Azuma et al. in view of Bonaccio et al., and further in view of Min et al. (U.S. Patent No. 6,515,489), for the reasons substantially of record.

Claim 4 depends directly from amended independent claim 2, claim 5 depends from amended independent claim 3, and Min et al. does not remedy the deficiency of Azuma et al. and Bonaccio et al. Therefore, claims 4 and 5 are patentable over Azuma et al. and Bonaccio et al., even when considered in view of Min et al. Consequently, the allowance of claims 4 and 5 is respectfully solicited.

CONCLUSION

In view of the above amendment, Applicants believes the pending application is in condition for allowance.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Edward J. Wise (Reg. No. 34,523) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37.C.F.R. §§ 1.16 or 1.14; particularly, extension of time fees.

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Respectfully submitted,

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